WHAT IS CLAIMED IS:

1. A differential-to-single-ended (DSE) converter capable of receiving a positive differential input signal and a negative differential input signal and generating a single-ended output signal, said DSE converter comprising:

a first comparator having a non-inverting input coupled to said positive differential input signal and an inverting input coupled to said negative differential input signal;

a second comparator having an inverting input coupled to said positive differential input signal and a non-inverting input coupled to said negative differential input signal;

a first D flip-flop having an input connected to Logic 1 and clocked by a rising edge on an output of said first comparator;

a second D flip-flop having an input connected to Logic 1 and clocked by a rising edge on an output of said second comparator; and

a latch circuit having a first input coupled to an output of said first D flip-flop and a second input coupled to an output of said second D flip-flop, wherein a rising edge on an output of said first D flip-flop causes an output of said latch to change state and a rising edge on an output of said second D flip-flop causes said latch output to change state.

2. The differential-to-single-ended (DSE) converter as set forth in Claim 1, wherein said latch circuit comprises a first NOR gate having a first input coupled to said output of said first D flip-flop, a second input, and an output.

3. The differential-to-single-ended (DSE) converter as set forth in Claim 2, wherein said latch circuit comprises a second NOR gate having a first input coupled to said output of said second D flip-flop, a second input coupled to said first NOR gate output, and an output coupled to said second input of said first NOR gate.

4. The differential-to-single-ended (DSE) converter as set forth in Claim 3, wherein said first NOR gate is coupled to said first D flip-flop output by a first OR gate having a first input coupled to said first D flip-flop output, a second input coupled to Logic 0, and an output coupled to said first input of said first NOR gate.

5. The differential-to-single-ended (DSE) converter as set forth in Claim 4, wherein said first NOR gate output is coupled to a reset input of said first D flip-flop.

6. The differential-to-single-ended (DSE) converter as set forth in Claim 5, wherein said first NOR gate output is coupled to said reset input of said first D flip-flop via a buffer circuit.

7. The differential-to-single-ended (DSE) converter as set forth in Claim 4, wherein said second NOR gate output is coupled to a reset input of said second D flip-flop.

8. The differential-to-single-ended (DSE) converter as set forth in Claim 7, wherein said second NOR gate output is coupled to said reset input of said second D flip-flop via a buffer circuit.

9. The differential-to-single-ended (DSE) converter as set forth in Claim 1, wherein a speed of said first comparator is determined by a biasing current of said first comparator and said biasing current is adjustable to match a frequency of said positive and negative differential input signals.

10. The differential-to-single-ended (DSE) converter as set forth in Claim 1, wherein a speed of said second comparator is determined by a biasing current of said second comparator and said biasing current is adjustable to match a frequency of said positive and negative differential input signals.

11. A phase-locked loop (PLL) circuit comprising:

a voltage-controlled oscillator capable of receiving a control voltage and outputting a differential signal having a frequency controlled by said control voltage, said voltage-controlled oscillator comprising a ring oscillator containing a chain of delay cells having differential inputs and differential outputs;

a differential-to-single-ended (DSE) converter capable of receiving a positive differential input signal and a negative differential input signal from said voltage controlled oscillator and generating a single-ended output signal, said DSE converter comprising:

a first comparator having a non-inverting input coupled to said positive differential input signal and an inverting input coupled to said negative differential input signal;

a second comparator having an inverting input coupled to said positive differential input signal and a non-inverting input coupled to said negative differential input signal;

a first D flip-flop having an input connected to Logic 1 and clocked by a rising edge on an output of said first comparator;

a second D flip-flop having an input connected to Logic 1 and clocked by a rising edge on an output of said second comparator; and

a latch circuit having a first input coupled to an output of said first D flip-flop and a second input coupled to an output of said second D flip-flop, wherein a rising edge on an output of said first D flip-flop causes an output of said latch to change state and a rising edge on an output of said second D flip-flop causes said latch output to change state.

12. The phase-locked loop (PLL) circuit as set forth in Claim 11, wherein said latch circuit comprises a first NOR gate having a first input coupled to said output of said first D flip-flop, a second input, and an output.

13. The phase-locked loop (PLL) circuit as set forth in Claim 12, wherein said latch circuit comprises a second NOR gate having a first input coupled to said output of said second D flip-flop, a second input coupled to said first NOR gate output, and an output coupled to said second input of said first NOR gate.

14. The phase-locked loop (PLL) circuit as set forth in Claim 13, wherein said first NOR gate is coupled to said first D flip-flop output by a first OR gate having a first input coupled to said first D flip-flop output, a second input coupled to Logic 0, and an output coupled to said first input of said first NOR gate.

15. The phase-locked loop (PLL) circuit as set forth in Claim 14, wherein said first NOR gate output is coupled to a reset input of said first D flip-flop.

16. The phase-locked loop (PLL) circuit as set forth in Claim 15, wherein said first NOR gate output is coupled to said reset input of said first D flip-flop via a buffer circuit.

17. The phase-locked loop (PLL) circuit as set forth in Claim 14, wherein said second NOR gate output is coupled to a reset input of said second D flip-flop.

18. The phase-locked loop (PLL) circuit as set forth in Claim 15, wherein said second NOR gate output is coupled to said reset input of said second D flip-flop via a buffer circuit.

19. The phase-locked loop (PLL) circuit as set forth in Claim 11, wherein a speed of said first comparator is determined by a biasing current of said first comparator and said biasing current is adjustable to match a frequency of said positive and negative differential input signals.

20. The phase-locked loop (PLL) circuit as set forth in Claim 11, wherein a speed of said second comparator is determined by a biasing current of said second comparator and said biasing current is adjustable to match a frequency of said positive and negative differential input signals.